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DATE: Monday, April 12, 2004

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☐	L54	L53 and (hdl or vhdl) and simula$ and (synthes$ or design$)	1
☐	L53	l1 and L52	56
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☐	L51	L50 and l1	3
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☐	L44	L43 and (hdl or vhdl)	0
☐	L43	L41 and relation$ and (simula$ or synthes$ or design$)	35
☐	L42	L41 and synthes$ and simulat$ and (hdl or vhdl or verilog or programm$)	2
☐	L41	L40 and l1 and l14	44
☐	L40	compil$ same intermedia$ same code	1662
☐	L39	l1 and l27	5
☐	L38	L37 and l1	2
☐	L37	L36 and port and buffer and (flip adj flop)	23
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☐	L2	L1 and hdl and synthes$ and simulat$	13
☐	L1	boolean same object	2605

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 20030216901 A1

Using default format because multiple data bases are involved.

L38: Entry 1 of 2   File: PGPB   Nov 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030216901
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030216901 A1

TITLE: Design apparatus and a method for generating an implementable description of
a digital system

PUBLICATION-DATE: November 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Schaumont, Patrick	Wijgmaal		BE	
Vernalde, Serge	Heverlee		BE	
Cockx, Johan	Pellenberg		BE	

US-CL-CURRENT: 703/13

☐ 2. Document ID: US 6606588 B1

L38: Entry 2 of 2   File: USPT   Aug 12, 2003

US-PAT-NO: 6606588
DOCUMENT-IDENTIFIER: US 6606588 B1

TITLE: Design apparatus and a method for generating an implementable description of
a digital system

Terms	Documents

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Search Results - Record(s) 1 through 6 of 6 returned.

☐ 1. Document ID: US 20030216901 A1

Using default format because multiple data bases are involved.

L48: Entry 1 of 6   File: PGPB   Nov 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030216901
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030216901 A1

TITLE: Design apparatus and a method for generating an implementable description of a digital system

PUBLICATION-DATE: November 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Schaumont, Patrick	Wijgmaal		BE	
Vernalde, Serge	Heverlee		BE	
Cockx, Johan	Pellenberg		BE	

US-CL-CURRENT: 703/13

☐ 2. Document ID: US 20020080174 A1

L48: Entry 2 of 6   File: PGPB   Jun 27, 2002

PGPUB-DOCUMENT-NUMBER: 20020080174
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020080174 A1

TITLE: System and method for configuring an instrument to perform measurement functions utilizing conversion of graphical programs into hardware implementations

PUBLICATION-DATE: June 27, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kodosky, Jeffrey L.	Austin	TX	US	
Andrade, Hugo	Austin	TX	US	

Odom, Brian Keith   Georgetown   TX   US
Butler, Cary Paul   Austin   TX   US
Schultz, Kevin L.   Georgetown   TX   US

US-CL-CURRENT: <u>345</u>/<u>762</u>

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 3. Document ID: US 6608638 B1

L48: Entry 3 of 6   File: USPT   Aug 19, 2003

US-PAT-NO: 6608638
DOCUMENT-IDENTIFIER: US 6608638 B1

TITLE: System and method for configuring a programmable hardware instrument to perform measurement functions utilizing estimation of the hardware implentation and management of hardware resources

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 4. Document ID: US 6606588 B1

L48: Entry 4 of 6   File: USPT   Aug 12, 2003

US-PAT-NO: 6606588
DOCUMENT-IDENTIFIER: US 6606588 B1

TITLE: Design apparatus and a method for generating an implementable description of a digital system

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 5. Document ID: US 6584601 B1

L48: Entry 5 of 6   File: USPT   Jun 24, 2003

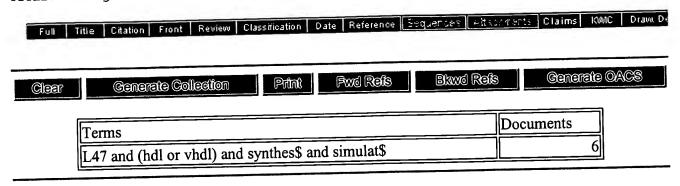US-PAT-NO: 6584601
DOCUMENT-IDENTIFIER: US 6584601 B1

TITLE: System and method for converting graphical programs into hardware implementations which utilize probe insertion

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 6. Document ID: US 6457164 B1

L48: Entry 6 of 6   File: USPT   Sep 24, 2002

US-PAT-NO: 6457164
DOCUMENT-IDENTIFIER: US 6457164 B1

TITLE: Hetergeneous method for determining module placement in FPGAs

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

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Terms	Documents
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